Your Comments Please

HP E2432A

Your comments assist us in meeting your needs better. Please complete this questionnaire and return it to us. Feel free to add any additional comments that you might have. All comments and suggestions become the property of Hewlett-Packard. Omit any questions that you feel would be proprietary.

	Yes	No
1. Did you receive your product when expected?	[ ]	[ ]
2. Were you satisfied with the operation of the preprocessor interface at turn-on?	[ ]	[ ]

3. Were the proper accessories supplied with your product?

If not, what was missing?

Cables [ ] Manual(s) [ ] Other _____

4. What measurements will this preprocessor interface be used to make?

_____

5. Which logic analyzer are you using?

Type_____

6. What do you like most about the preprocessor interface? _

_____

7. What would you like to see changed or improved?_____

8. Which sections of the manual(s) have you used?

[ ] Installation Overview
[ ] Step-By-Step Procedures
[ ] Characteristics

9. Please rate the manual(s) on the following:

4= Excellent 3= Good 2= Adequate 1= Poor

[ ] Breadth and depth of information
[ ] Ability to easily find information
[ ] Ability to understand and apply the information provided in the manual

Please explain:_____

10. What is your experience with logic analyzers and preprocessor interfaces?

[ ] No previous experience
[ ] Less than 1 year experience
[ ] More than 1 year's experience on one model
[ ] More than 1 year's experience on several models

Name _____ Company _____

Address _____ Zip Code _____

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THANK YOU FOR YOUR HELP

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HP 1650A/B and HP 1651A/B

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Zusatzinformation für Meß- und Testgeräte

Werden Meß- und Testgeräte mit ungeschirmten Kabeln und/oder in offenen Meßaufbauten verwendet, so ist vom Betreiber sicherzustellen, daß die Funk-Entstörbestimmungen unter Betriebsbedingungen an seiner Grundstücksgrenze eingehalten werden.

Manufacturer's declaration

This is to certify that this product HP 1650A/B and HP 1651A/B meets the radio frequency interference requirements of directive Vfg. 1046/84. The German Bundespost has been notified that this equipment was put into circulation and was granted the right to check the product type for compliance with these requirements.

Additional Information for Test- and Measurement Equipment

Note: If test and measurement equipment is operated with unshielded cables and/or used for measurements on open set-ups, the user must insure that under these operating conditions, the radio frequency interference limits are met at the border of his premises.

Note: This declaration indicates compliance of this product with the German RFI specifications stated in the German Vfg. 1046/84 directive.

HP E2432A Intel 80960CA/CF Preprocessor Interface User's Guide

for the HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers

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A software code may be printed before the date; this indicates the version of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one to one correspondence between product updates and manual updates.

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The List of Effective Pages gives the date of the current edition and of any pages changed in updates to that edition. Within the manual, any page changed since the last edition is indicated by printing the date the changes were made on the bottom of the page. If an update is incorporated when a new edition of the manual is printed, the change dates are removed from the bottom of the pages and the new edition date is listed in the Printing History and on the title page.

Pages	**Effective Date**

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This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this user's guide must be heeded.

Contents

Chapter 3: General Information

Appendix A: Troubleshooting

Introduction

The HP E2432A Preprocessor Interface provides a complete interface for state analysis between any 80960CA/CF target system and the following logic analyzers: HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, and HP 16550A.

The 80960CA/CF configuration software on the flexible disk sets up the format specification menu of the logic analyzer for compatibility with the 80960CA/CF microprocessor. It also provides the inverse assembler for obtaining displays of 80960CA/CF data in 80960CA/CF assembly language mnemonics.

The HP E2432A Preprocessor Interface can be used together with the HP E2410A Universal Interface for intermodule measurements, to provide both state and timing analysis. For information on the Universal Interface, refer to the *HP E2410A Universal Interface User's Guide.*

Logic Analyzer Software Compatibility

The HP E2432A Preprocessor Interface requires HP 16500A system software version V04.01 or higher (for the HP 16550A Logic Analyzer, version V05.01 or higher is required). If your software version is older than V04.01, load new HP 16500A system software with a version number of V04.01 or higher before loading the HP E2432A software. For HP 1660-series logic analyzers, software version V01.00 or higher is required.

Logic Analyzers Supported

The following logic analyzers are supported by the HP E2432A Preprocessor Interface:

HP 1650A, HP 1650B, HP 1652B, HP 16510A, and HP 16510B

These logic analyzers provide 1 k of memory depth with either 80 channels of 35 MHz state analysis (25 MHz state analysis for the HP 1650A or HP 16510A) or 80 channels of 100 MHz timing analysis.

HP 1660A/61A

The HP 1660A/61A Logic Analyzers provide 4 k of memory depth with 136 channels (HP 1660A) or 102 channels (HP 1661A) of 100 MHz state analysis or 250 MHz timing analysis. These logic analyzers also support various combinations of mixed state/timing analysis.

HP 16511B

This logic analyzer combination provides 1 k of memory depth with either 160 channels of 35 MHz state analysis, or 80 channels of 35 MHz state analysis and 80 channels of 100 MHz timing analysis.

HP 16540A,D with two HP 16541A,D Expansion Cards

This logic analyzer combination provides 4 k of memory depth (16 k with the D version) with 112 channels of 100 MHz state or timing analysis.

HP 16542A (Master Card and four expansion cards)

This logic analyzer combination provides 1 M of memory depth with 80 channels of 100 MHz state or timing analysis.

HP 16550A (one or two cards)

This logic analyzer provides 4 k of memory depth with 102 channels per card of 100 MHz state analysis or 250 MHz timing analysis. It also supports various combinations of mixed state/timing analysis.

The 80-channel logic analyzers and the HP 1661A provide 32 Address lines, 32 Data lines, and 16 key microprocessor Status signals. The HP 16540/16541A,D, HP 16550A (two cards), HP 1660A, and HP 16511B Logic Analyzers additionally provide all Interrupt Controller signals, all DMA Controller signals, and the remaining microprocessor Status signals.

How to Use This Manual

This manual is organized into three chapters and one appendix:

- Chapter 1 explains how to install and configure the HP E2432A Preprocessor Interface for state analysis with the supported logic analyzers. It also explains how to initialize the inverse assembler.
- Chapter 2 provides reference information on the format specification and symbols configured by the HP E2432A software. It also provides further information about the inverse assembler and status encoding.
- Chapter 3 contains additional reference information including the characteristics and signal mapping for the HP E2432A Preprocessor Interface. It also contains information on servicing.
- Appendix A contains information on troubleshooting problems or difficulties which may occur with the preprocessor interface.

1

Setting Up the HP E2432A

Introduction

This chapter explains how to install and configure the HP E2432A Preprocessor Interface for state analysis with the supported logic analyzers.

Duplicating the Master Disk

Before you use the HP E2432A software, use the Duplicate Disk operation in the disk menu of your logic analyzer to make a duplicate copy of the HP E2432A master disk. Store the master disk and use the back-up copy to configure your logic analyzer. This will help prevent the possibility of losing or destroying the original files in the event the disk wears out, is damaged, or a file is accidentally deleted.

Equipment Supplied

The HP E2432A Preprocessor Interface consists of the following equipment:

- The preprocessor interface hardware, which includes the preprocessor interface circuit card and cables.
- The configuration files and inverse assembly software on a 3.5-inch disk.
- Seven 100 kOhm Termination Modules (HP part number 01650-63204)
- This user's guide.

Note

The preprocessor interface socket assembly pins are covered at the time of shipment with a protective foam pad. This is done to protect the delicate gold-plated pins of the assembly from damage due to impact. When you're not using the preprocessor interface, protect the socket assembly pins from damage by covering them with the foam protector.

Minimum Equipment Required

The minimum hardware for state analysis of an 80960CA/CF target system consists of the following equipment:

- An HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540/16541A,D, HP 16542A, or HP 16550A Logic Analyzer.
- The 80960CA/CF Preprocessor Interface and Inverse Assembler (HP E2432A).

Installation Quick Reference

The following procedure describes the major steps required to perform measurements with the HP E2432A Preprocessor Interface. The page numbers listed in the various steps refer you to sections in this manual that offer more detailed information.

Caution 

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Set the Clock Jumper according to which logic analyzer you are using (see table 1-1 on page 1-3).
2. Set the four 8-bit DIP switches on the preprocessor interface. These settings must match the programmed 80960CA/CF Memory Region Configuration Table for READY# /BTERM# and bus pipeline enabling (see page 1-4).
3. Connect the 100 kOhm Termination Modules to the cables on the preprocessor interface (see page 1-6).
4. Install the preprocessor interface in the target system (page 1-7).
5. Connect the logic analyzer probe cables to the termination modules on the cable connectors of the preprocessor interface board as listed in table 1-2. Some of the logic analyzers have more than one configuration file and connections, according to whether you want to probe the interrupts or the DMA signals. See pages 1-10 and 1-11.

6. Apply power to the logic analyzer, and then to your target system. The logic analyzer must be powered up first, since it supplies power to the preprocessor interface.

7. Load the logic analyzer configuration file for the logic analyzer you are using (see page 1-8). Table 1-2 lists the configuration files along with the connections for the various logic analyzers. Loading the configuration file also automatically loads the inverse assembler.

8. Initialize the inverse assembler, to match the 80960CA/CF Memory Region Configuration Table (see page 1-12).

9. If you want to fully capture the execution trace, disable the cache memory. If you leave the cache enabled, all states will still be captured and decoded but you may lose some of the execution trace.

You are now ready to make measurements with the preprocessor interface.

Setting the Clock Jumper

Connector J1 on the preprocessor interface circuit board changes the Setup/Hold times to meet the requirements for various logic analyzers. Table 1-1 shows the required connections according to which logic analyzer you are using. Figure 1-1 shows the location of J1.

Table 1-1. Jumper J1 Connections

Logic Analyzer	Setup/Hold Required by Logic Analyzer	Maximum 80960CA/CF Bus Rate Supported	Jumper J1 Pins
HP 1650A or 16510A	10 ns setup/0 s hold	25 MHz	2 and 3
HP 1650B, 1652B, 16510B, or 16511B	10 ns setup/0 s hold	35 MHz	2 and 3
HP 16540/16541A,D, HP 16542A	4 ns setup/0 s hold	40 MHz	1 and 2
HP 16550A, HP 1660A/61A	3.5 ns setup/0 s hold	40 MHz	1 and 2

Setting Up the Memory Region Configuration Switches

The preprocessor interface must be configured to match the programmed 80960CA/CF Memory Region Configuration Table (MRCT) of the target system. If you later change the 80960CA/CF MRCT, you must also change the switches.

There are four 8-bit DIP switches on the preprocessor interface circuit board, labeled S1 - S4 (see figure 1-1). The top two DIP switches are for READY# /BTERM# enabling (S3 and S4), and the bottom two are for bus pipeline enabling (S1 and S2). The switch pairs correspond to the 16 Memory Regions in the 80960CA/CF. The left-most bit is for region 15, and the right-most bit is for region 0, as shown in figure 1-1.

When a switch is in the up position, the preprocessor interface is enabled to use READY# /BTERM# or bus pipelining in that region. When a switch is down, it disables the region. The switches do not affect the operation of the 80960CA/CF; they only affect how the preprocessor interface samples the microprocessor bus.

Note 

The preprocessor interface must be configured exactly the same as the 80960CA/CF MRCT or incorrect sampling may occur.

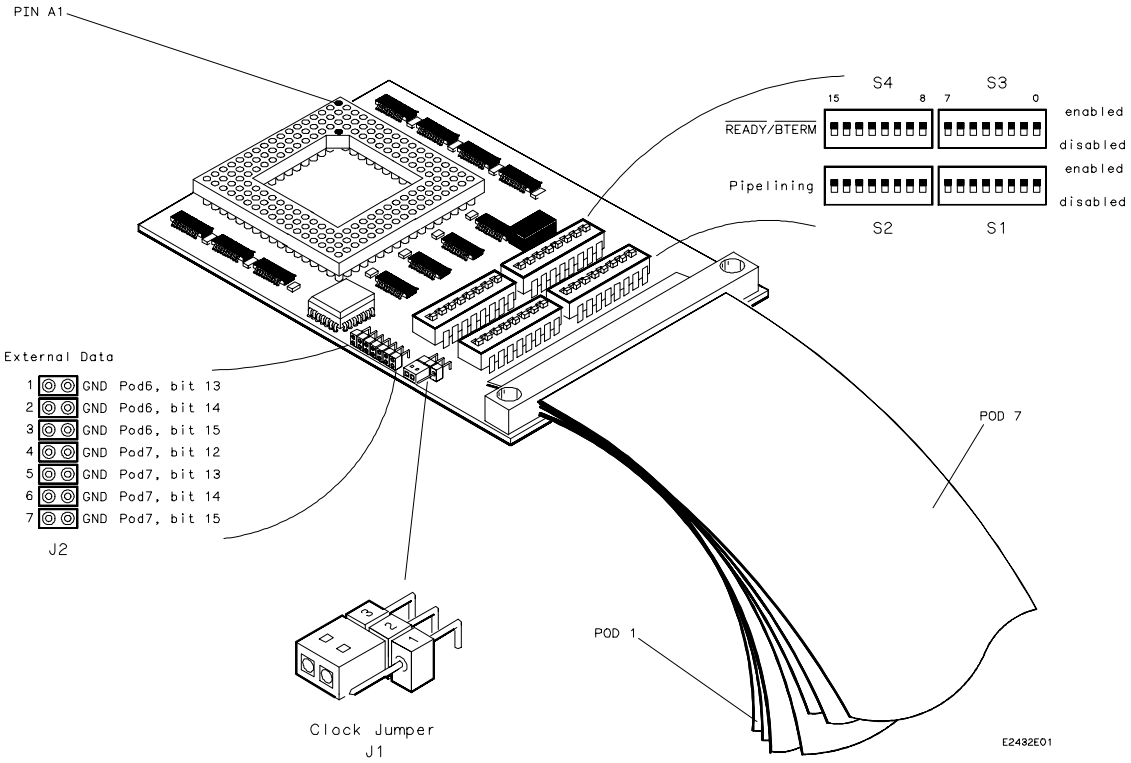

Figure 1-1. Preprocessor Interface Assembly

Caution Care must be used when removing a microprocessor or socket from the preprocessor interface board to prevent damaging the circuit traces.

Connecting the Termination Module to the Preprocessor Interface

The 100 kOhm Termination Module (HP part number 01650-63204) properly terminates the logic analyzer probes. The following steps explain how to connect the termination module to the cables on the HP E2432A Preprocessor Interface:

1. Align the key on the female end of the termination module with the slot on the connector of one of the preprocessor interface cables.
2. Push the termination module into the connector.
3. Repeat steps 1 and 2 for each termination module.

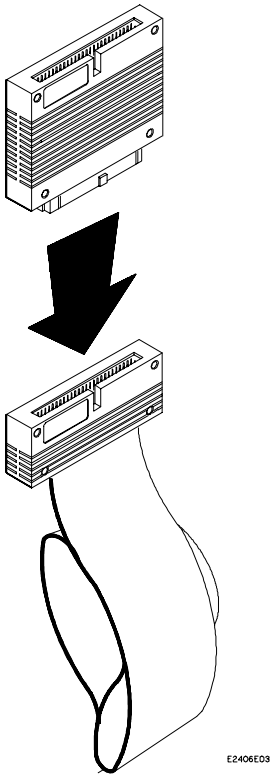

Figure 1-2. Connecting the Termination Module

Connecting to the Target System

The following steps explain how to connect the HP E2432A Preprocessor Interface to your target system:

Caution

To prevent equipment damage, be sure to remove power from both the logic analyzer and the target system whenever the preprocessor interface or microprocessor is being connected or disconnected.

1. Remove the 80960CA/CF microprocessor from its socket on the target system and store it in a protected environment.

Caution

Serious damage to the target system or preprocessor interface can result from incorrect connection. Note the position of pin A1 (figure 1-1) on the preprocessor interface connector and the target system socket prior to inserting the connector in the socket. Also, take care to align the preprocessor interface connector with the socket on the target system so that all microprocessor pins are making contact.

2. Plug the preprocessor interface connector into the microprocessor socket on the target system.

Note

If the preprocessor interface connector interferes with components of the target system or if a higher profile is required, additional plastic pin protectors/extenders can be added. Plastic pin protectors/extenders can be ordered from Hewlett-Packard using the part number 1200-1512. However, any 168-pin PGA IC socket with an 80960CA/CF footprint and gold-plated pins can be used.

3. Plug the 80960CA/CF microprocessor into the socket of the preprocessor interface board. The socket on the preprocessor interface board is designed with low-insertion-force pins to allow you to install or remove the microprocessor with minimum force.

4. Apply power to the logic analyzer first, and then to your target system. The logic analyzer must be powered up first, since it supplies power to the preprocessor interface.

Connecting to the HP E2432A

Connect the logic analyzer probes to the termination modules on the cable connectors of the preprocessor interface board as listed in table 1-2 (pages 1-10 and 1-11). Some of the configurations allow you to probe either the interrupts or the DMA signals.

Figure 1-3 shows the relative locations for the logic analyzer cards.

Power Up / Down Sequence

When powering up, the logic analyzer must be powered up first, and then the target system. The logic analyzer provides the power to the active circuits on the preprocessor interface; unpowered circuits may cause improper operation of the target system.

When powering down, the target system should be powered down first, and then the logic analyzer.

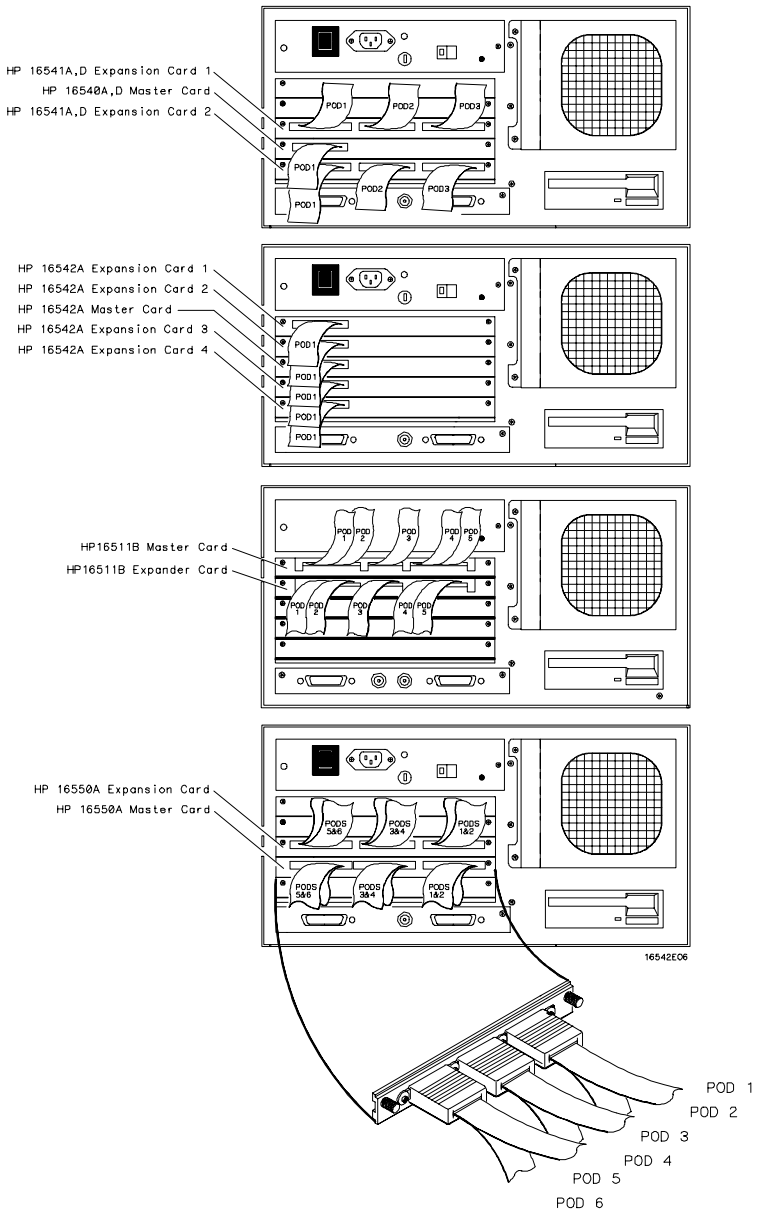

Figure 1-3. Logic Analyzer Card Locations (relative locations, actual slots used may vary)

Table 1-2. Logic Analyzer Connections and Configuration Files (HP 1650 series, HP 16510A/B, HP 16511B, HP 16540/16541A,D, HP 16550A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 1650A/B, HP 1652B, HP 16510A/B	PI960CA_01		P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P1 STAT_1 clk ⇕
HP 16511B Upper Card	PI960CA_02		P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P1 STAT_1 clk ⇕
HP 16511B Lower Card			--	--	--	P7 STAT_3	P6 STAT_2
HP 16541A,D Exp. Card 1	PI960CA_03				P7 STAT_3	P5 ADDR_H	P4 ADDR_L
HP 16540A,D Master Card							P1 STAT_1 clk ⇕
HP 16541A,D Exp. Card 2					P6 STAT_2	P3 DATA_H	P2 DATA_L
HP 16550A Exp. Card	PI960CA_06	--	--	--	--	--	P7 STAT_3
HP 16550A Master Card		P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P6 STAT_2	P1 STAT_1 clk ⇕
HP 16550A	PI960CA_05 (probes DMA)	P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P7 STAT_3	P1 STAT_1 clk ⇕
HP 16550A	PI960CA_04 (probes Interrupts)	P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P6 STAT_2	P1 STAT_1 clk ⇕

Table 1-2. Logic Analyzer Connections and Configuration Files (HP 1660 series, HP 16542A)

Logic Analyzer	File	Pod 6	Pod 5	Pod 4	Pod 3	Pod 2	Pod 1
HP 16542A Exp. Card 1	PI960CA_03						P5 ADDR_H
HP 16542A Exp. Card 2							P4 ADDR_L
HP 16542A Master Card							P1 STAT_1 clk ⇳
HP 16542A Exp. Card 3							P3 DATA_H
HP 16542A Exp. Card 4							P2 DATA_L
HP 1660A	PI960CA_03	**(Pod 6)** P5 ADDR_H **(Pod 7)** P7 STAT_3	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P6 STAT_2	P1 STAT_1 clk ⇳
HP 1661A	PI960CA_03 (probes DMA)	P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P6 STAT_2	P1 STAT_1 clk ⇳
HP 1661A	PI960CA_05 (probes Interrupts)	P5 ADDR_H	P4 ADDR_L	P3 DATA_H	P2 DATA_L	P7 STAT_3	P1 STAT_1 clk ⇳

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for 80960CA/CF state analysis by loading the appropriate 80960CA/CF configuration file for the logic analyzer. Loading the configuration file also loads the inverse assembler. To load the configuration file and inverse assembler:

1. Install the HP E2432A flexible disk in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP 1650 series logic analyzers, select the I/O Disk Operations menu.
   - For the HP 1660 series and HP 16500 series logic analyzers, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer configuration from disk.
4. For HP 16500-series and HP 1660-series logic analyzers, select the appropriate module (such as "100/500 MHz LA" or "Analyzer") for the load.
5. Use the knob to select the appropriate configuration file (see table 1-2), depending on which logic analyzer is being used.
6. Execute the load operation to load the file into the logic analyzer.

Initializing the Inverse Assembler

In order to disassemble 80960CA/CF code, the HP E2432A Inverse Assembler must first be initialized. During initialization, the inverse assembler extracts the target Memory Region Configuration Table (MRCT) for byte order and bus size information in each of the 16 memory regions. The states must be examined from RESET up through the MRCT.

Once the inverse assembler is initialized, it will remember the byte order and bus size information for each region. If the logic analyzer is turned off, or a new 80960CA/CF MRCT is loaded, the inverse assembler must be reloaded and re-initialized.

To initialize the inverse assembler, use the following procedure:

1. Load the logic analyzer configuration file; this will automatically load the inverse assembler. Each time you load a configuration file which has an inverse assembler attached, the inverse assembler must be initialized (see page 1-15 for information on attached inverse assemblers).

2. Enable the Trigger/Trace Specification Menu, and set it to:
   (1) While storing "no state" TRIGGER on "a" 1 times
   (2) Store "≠ b"
   Pattern "b" is Label ADS set to "ADDR CYCLE", as shown in figure 1-4. This is the default Trace Specification which is supplied in the logic analyzer configuration files.

3. Run the logic analyzer, and execute a hardware RESET on the 80960CA/CF. A software RESET is not sufficient. You should see a listing similar to that shown in figure 1-5.

4. Scroll the listing on the logic analyzer display until you see the message "Extracting Region Configuration Info" (you may have to scroll through over 100 state listing lines). When you see this message, the inverse assembler is initialized, and you are now ready to make further measurements.

The inverse assembler must be reinitialized each time you reload it. It will remain correctly initialized as long as the logic analyzer is powered up and the 80960CA/CF MRCT remains unchanged.

After this process is complete, you can clear the trigger/trace specification and set it up for your measurement requirements.

Saving a RESET Configuration

For some target systems or measurements it may be difficult or undesirable to execute a hardware RESET. You can avoid steps 1 through 3 above by saving a configuration file which contains the MRCT information. When you later load this configuration file, all you need to do is scroll the display (step 4), and the inverse assembler will be initialized for that MRCT.

To store a configuration file with the MRCT data, follow steps 1 through 3 above, then save the configuration file under another name, such as RSTCONF. You can then use RSTCONF for any future measurements with the same logic analyzer and MRCT. You can also store a configuration file which contains measurement data, so that you can later re-examine the data (see page 1-15).

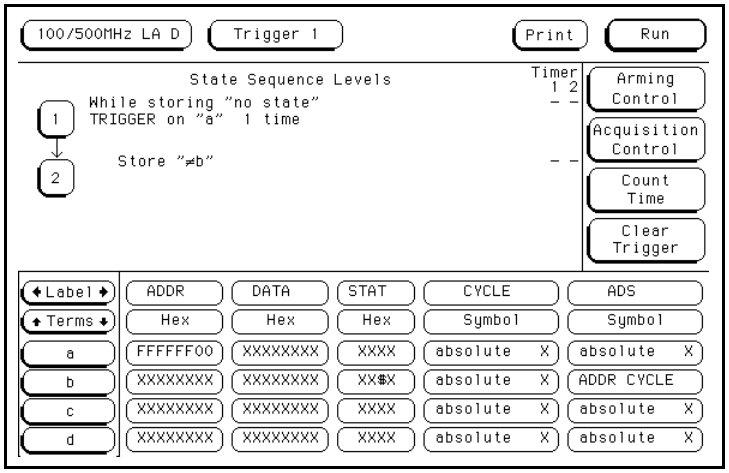

Figure 1-4. Trigger/Trace Specification Menu

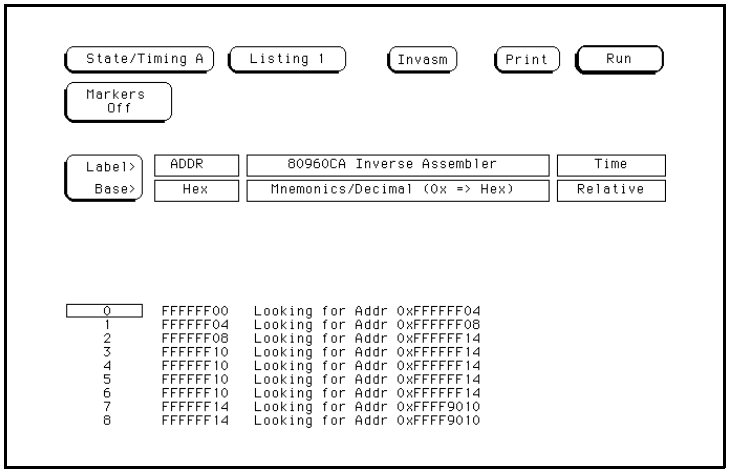

Figure 1-5. RESET Listing

Examining Stored Data

In some instances you may want to store data from a measurement, and examine that data at a later time. However, when you reload the configuration file with the stored data, the inverse assembler will also be reloaded, but it will no longer be initialized and the data will not disassemble. If you re-initialize the inverse assembler, the stored data will be lost.

To view this stored data, you will have to unattach the inverse assembler from the configuration file, so that you can initialize the inverse assembler and then load the configuration file separately.

To view stored data, use the following procedure:

1. Rename the inverse assembler file. The easiest way is to change the I to an X, so that it is named XA960CA_PI. This will remove the name IA960CA_PI from the list of files.

2. Load in the configuration file with the stored data. The configuration file will look for the inverse assembler, and not find it. You should get the following message: "File not found, 80960CA/CF: "IA960CA_PI" inverse assembler not found."

3. Store this configuration file back to the disk, using its same filename. Since the inverse assembler could not be found, the configuration file is stored without the inverse assembler attached.

4. Rename the inverse assembler back to IA960CA_PI.

5. Load in the original configuration file for the logic analyzer (without the stored data), or use the RSTCONF for that MRCT, as mentioned on page 1-13. This will also load the inverse assembler.

6. Initialize the inverse assembler, as described on pages 1-12 and 1-13.

7. Reload from the disk the configuration file with the stored data. Since this configuration file no longer has an attached inverse assembler, the initialized inverse assembler from steps 5 and 6 will remain in the logic analyzer memory.

You are now ready to view the stored data.

Connecting External Signals

You can connect up to seven additional signals from your target system to the preprocessor interface. These external signals are sampled synchronously with the 80960CA/CF data signals. The state of these signals can be viewed in the EXTERN label in the format specification. Chapter 3 contains the signal-to-connector mapping tables.

Since these labels are on pods 6 and 7, they can only be viewed on logic analyzers which have more than 80 channels. Figure 1-1 (page 1-5) shows the connection points for these signals. Each signal has one connection point for the signal and a corresponding connection point for the ground.

Using the Preprocessor Interface with the Universal Interface

The HP E2432A Preprocessor Interface can be used together with the HP E2410A Universal Interface to perform intermodule measurements with HP 16500A Logic Analysis Systems. The basic functions of the HP 16500A Intermodule menu give you the ability to do the following:

- Configure modules to run simultaneously.
- Set up arming sequences between modules.
- Adjust skew between modules.
- Synchronize with external equipment.
- Display resulting waveforms and state listings for several modules on one screen.

To use the preprocessor interface together with the universal interface, first install the preprocessor interface in the 80960CA/CF microprocessor socket, and then install the universal interface on top of the preprocessor interface. The 80960CA/CF microprocessor is then installed on top of the universal interface. Connect the Termination Modules/Adapters and the logic analyzer probe cables. Load the appropriate configuration files into the logic analyzers, and use the Intermodule Measurements menu (in the System field) to make measurements.

For a detailed description of intermodule measurements and using the Intermodule Measurements menu, refer to the *HP 16500A Installation/Operation Reference Manual*, or the *HP E2433-60002 Training Kit for the HP Logic Analyzers*.

2

Analyzing the Intel 80960CA/CF

Introduction

This chapter provides reference information on the format specification and symbols configured by the HP E2432A software. It also provides information about the inverse assembler and status encoding.

Format Specification

The HP E2432A software sets up format specifications for the logic analyzers. There will be some slight differences in the displays, according to which logic analyzer you are using. For example, some logic analyzers do not have a Clock Period field. Refer to your logic analyzer manual to see which fields and displays are available.

Table 3-1 in chapter 3 lists the 80960CA/CF signals for the HP E2432A Preprocessor Interface and their corresponding lines to the logic analyzer.

Maximum Frequencies for Clock Period > 60 ns

For most 80960CA/CF frequencies and modes of operation, the Clock Period in the Format menu of the logic analyzer should be set to > 60 ns (default setting). The only exceptions are for transactions where the bus rate is greater than 16.67 MHz (see table 2-1). If the bus rate is greater than 16.67 MHz, set the Clock Period field to < 60 ns. Time tagging is not available when the Clock Period is < 60 ns.

The HP 1660A/61A, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers do not have a Clock Period field. They operate at 100 MHz, which is above the maximum frequency of the Intel 80960CA/CF.

For more information on the Clock Period field, refer to the reference manual for your logic analyzer.

Table 2-1. Bus Rates

Microprocessor Speed	Wait States	Bus Rate	Clock Period Field
16 MHz	0	16 MHz	> 60 ns
25 MHz	0 1	25 MHz 12 MHz	< 60 ns > 60 ns
33 MHz	0 1	*33 MHz 16 MHz	< 60 ns > 60 ns
40 MHz	0 1 2	**40 MHz 20 MHz 13 MHz	not applicable < 60 ns > 60 ns

* Not applicable for HP 1650A and HP 16510A Logic Analyzers.
** Applicable only for HP 1660A/61A, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers.

Listing Menu

Captured data is displayed as shown in figure 2-1. This figure displays the state listing for 32-bit bus cycles after disassembly. The inverse assembler is constructed so the mnemonic output closely resembles the actual assembly source code.

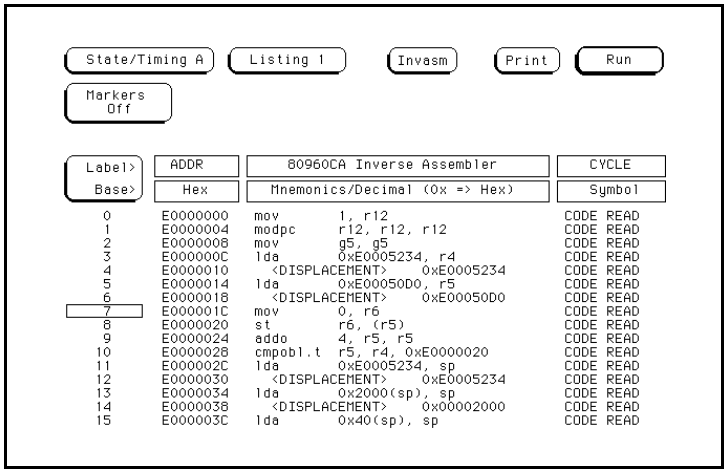

Figure 2-1. State Listing

Symbols

The configuration files set up labels and symbol tables in the logic analyzer. Symbols represent specific patterns within the labels which identify certain 80960CA/CF states or operations. The symbols are included to make it easier to recognize and trigger on specific 80960CA/CF states, and to make the listings more readable.

Table 2-2 lists the bits for the STAT label. Table 2-3 (pages 2-5 to 2-7) lists the symbols. The patterns for each symbol listed in the tables are shown in the binary base. In the actual configuration software, these patterns are listed in the hexadecimal base to conserve horizontal display space.

Table 2-2. STAT Label Bits

Bit	Status Signals	Description
0 - 3	BE0# - BE3#	These bits specify which bytes on the data bus are active during an access. The specific meanings vary depending on the bus width.
4	W/R#	This signal is high for write transactions and low for read transactions.
5	ADS#	This signal is low for a valid address cycle.
6	READY#	A low indicates that data is ready to transfer, in regions where READY# and BTERM# are enabled.
7	BTERM#	A low indicates that an access is to be terminated, in regions where READY# and BTERM# are enabled.
8	D/C#	This signal is high for a data access and low for a code access.
9	BLAST#	A low indicates the last transfer in an access.
10	LOCK#	A low indicates that the bus is locked.
11	HOLDA	A high indicates that the microprocessor is off the bus.
12	BREQ	A high indicates a microprocessor bus request.
13	DMA#	A low indicates that the access was initiated by the DMA controller.
14	SUP#	A low indicates that the access was initiated while in supervisor mode.
15	BOFF#	A low indicates that the microprocessor must get off the bus by the next clock cycle.

Table 2-3. Symbols

Label	Symbol	Bit Value
W/R	READ	0
	WRITE	1
ADS	ADDR CYCLE	0
	(blank)	1
READY	VALID DATA	0
	(blank)	1
BTERM	ACCESS ENDED	0
	(blank)	1
D/C	CODE	0
	DATA	1
BLAST	LAST XFER	0
	(blank)	1
LOCK	BUS LOCKED	0
	(blank)	1
HOLDA	(blank)	0
	PROC OFF BUS	1
BREQ	(blank)	0
	PROC BUS REQ	1
DMA	DMA ACCESS	0
	(blank)	1
SUP	SUP ACCESS	0
	(blank)	1
BOFF	BUS BACKOFF	0
	(blank)	1
HOLD	(blank)	0
	EXT BUS REQ	1
FAIL	IN PROG/FAIL	0
	STEST PASSED	1
STEST	STEST DISBLD	0
	STEST ENBLD	1
ONCE	ONCE ASSERTED	0
	(blank)	1
NMI	NONMASK INTR REQ	0
	(blank)	1

Table 2-3. Symbols (continued)

Label	Symbol	Bit Pattern
CYCLE (D/C# , W/R#)	CODE READ DATA READ DATA WRITE	0 0 1 0 1 1
BUS1 (HOLD, BREQ, HOLDA)	 HOLDA BREQ BREQ HOLDA HOLD HOLD HOLDA HOLD BREQ HOLD BREQ HOLDA	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1
BUS2 (BOFF# , SUP# , DMA#)	 DMA SUP SUP DMA BOFF BOFF DMA BOFF SUP BOFF SUP DMA	1 1 1 1 1 0 1 0 1 1 0 0 0 1 1 0 1 0 0 0 1 0 0 0
TESTS (STEST, FAIL#)	STEST DISBLD IN PROG/FAIL STEST PASSED	X 0 0 1 1 1
DREQ	DMA CH0 REQ DMA CH1 REQ DMA CH2 REQ DMA CH3 REQ NO DMA REQ	1 1 1 0 1 1 0 1 1 0 1 1 0 1 1 1 1 1 1 1

Table 2-3. Symbols (continued)

Label	Symbol	Bit Pattern
DACK	DMA CH0 ACK	1 1 1 0
	DMA CH1 ACK	1 1 0 1
	DMA CH2 ACK	1 0 1 1
	DMA CH3 ACK	0 1 1 1
	NO DMA ACK	1 1 1 1
EOP/TC	EOP0 OR TC0	1 1 1 0
	EOP1 OR TC1	1 1 0 1
	EOP2 OR TC2	1 0 1 1
	EOP3 OR TC3	0 1 1 1
	NO EOP/TC	1 1 1 1

The 80960CA/CF Inverse Assembler

The inverse assembler must be initialized to record the configuration information which is programmed in the 80960CA/CF Memory Region Configuration Table (MRCT). Chapter 1 contains information on how to initialize the inverse assembler.

The 80960CA/CF microprocessor does not provide enough status information for the inverse assembler to pick out the first word of two-word MEM type operations. To ensure correct disassembly for 8-bit and 16-bit accesses, you must put the first line of an opcode at the top of the display and press "Invasm." Once synchronized, the inverse assembler will disassemble from this point through the end of the screen. Use the following steps to synchronize the inverse assembler:

1. Select a line on the display that you know contains the beginning of an opcode.
2. Roll this line to the top of the screen.

Note 

The cursor location is not the top of the display. In figure 2-1, line 0 is the top of the display.

3. Select the "Invasm" field at the top of the display.
4. The listing will inverse assemble from the top line down. Any data before this display is left unchanged.

Rolling the display up will inverse assemble the lines as they appear on the bottom of the display. If you jump to another area of the display by entering a new line number, you may need to re-synchronize the inverse assembler by repeating steps 1 through 4.

Each time you inverse assemble a block of memory, the analyzer will keep that block in the inverse assembled condition. You can inverse assemble several different blocks in the analyzer memory, but activity between those blocks will not be inverse assembled.

Note

In order to get a screen display which more closely resembles an execution trace, you must disable the Instruction Cache. Otherwise, the inverse assembler disassembles only the code that is loaded in the Instruction Cache. During branches and jumps the listing may display instructions that were not executed by the program.

Interpreting Data

Numeric output from the inverse assembler is displayed in decimal unless it is prefixed by "0x." "0x" indicates hexadecimal notation.

The logic analyzers always probe the full 32-bit data bus of the 80960CA/CF. There are some memory transactions that use only 8, 16, or 24 bits of the data bus. The size of the bus cycle is indicated by the BE (Byte Enable) signals and the bus size configured in that memory region. If a particular byte of the data bus is not used, the inverse assembler marks these bits with "--." For example, in a 32-bit Little-Endian region, "0x--FF34--" indicates the following: hexadecimal notation, BE0 and BE3 are disabled, BE1 and BE2 are enabled, byte 1 has the value 34 hex, and byte 2 has the value FF hex.

Asterisks (**) indicate that there was insufficient information for the inverse assembler to disassemble completely.

If you leave the Instruction Cache enabled you may see displays of instructions that were not executed by the program When a program executes an instruction that causes a branch, the words after the branch in the Instruction Cache line fill are not used and will be discarded by the microprocessor. The logic analyzer captures all words as they are read into the Instruction Cache, even if they are not executed. Therefore, you may see displays of instructions that were not executed by the program.

Care must be taken when you are specifying a trigger condition or a storage qualification and the instruction of interest follows an instruction that may cause branching. An unused word may generate an unwanted trigger.

If you specify symbols for the ADDR label, these branch targets will show up in the inverse assembly listing as that ADDR symbol entry, instead of the default hex address. This allows the inverse assembly listing to more closely resemble the actual assembly source listing.

Note

Do not modify the ADDR, DATA, or STAT labels in the format specification if you want inverse assembly. Changes may cause incorrect results. Also note that if the trace specification is modified to store only selected bus cycles, incorrect or incomplete inverse assembly may result.

3

General Information

Introduction

This chapter contains additional reference information including the characteristics and signal mapping for the HP E2432A Preprocessor Interface.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the HP E2432A Preprocessor Interface. These characteristics are included as additional information for the user.

Microprocessor Compatibility: Intel 80960CA/CF and all microprocessors made by other manufacturers that comply with Intel 80960CA/CF specifications.

Microprocessor Package: 168-pin PGA.

Accessories Required: None.

Maximum Clock Speed: 40 MHz PCLK for the HP 1660A/61A, HP 16540/16541A,D, HP 16542A, and HP 16550A Logic Analyzers.
25 MHz PCLK for HP 1650A and HP 16510A Logic Analyzers.
33 MHz PCLK for all other logic analyzers.

Target Signal Timing: Meets all timing specifications as stated in *16-/32-bit Embedded Processors*, Intel 1991, Document # 270647-003, pages 4-65 and 4-66.

Signal Line Loading: One 74FCT load input on A28, A29, A30, PCLK1, and PCLK2.
ALE# , DT/R# , CLKIN, and CLKMODE are not probed, and therefore are not loaded.
One 74F load on all other lines.
All Vss tied together, and all Vcc and NC left open.

Power Requirements: 1.0 A at + 5 Vdc maximum, from the logic analyzer.

Logic Analyzer Required:	HP 1650A, HP 1650B, HP 1652B, HP 1660A/61A, HP 16510A, HP 16510B, HP 16511B, HP 16540A,D with two HP 16541A,D Expansion Cards, HP 16542A (Master Card and four expansion cards), or HP 16550A (one or two cards).	
Number of Probes Used:	Five, six, or seven 16-channel probes.	
Microprocessor Operations Displayed:	All bus transfers (normal, burst, pipeline, etc.) plus one cycle per HOLDA or BOFF# transaction.	
Environmental Temperature	Operating:	0 to + 55° C (+ 32 to + 131° F)
	Nonoperating:	-40 to + 75° C (-40 to + 167° F)
Altitude:	Operating:	4,600 m (15,000 ft)
	Nonoperating:	15,300 m (50,000 ft)
Humidity:	Up to 90% noncondensing. Avoid sudden, extreme temperature changes which could cause condensation within the instrument.	

Interface Description

The primary functions of a preprocessor interface are to connect the target microprocessor to the logic analyzer, and to perform any functions unique to that particular microprocessor. The HP E2432A Preprocessor Interface performs these functions in the following ways:

- By providing the required Setup/Hold times for the logic analyzer.
- By latching the address, status, and data bus of the 80960CA/CF microprocessor so that address, status, and data can be sent to the logic analyzer at the same time.
- By filtering out non-data transfer states (such as wait and idle).
- By generating the logic analyzer clocks from the appropriate 80960CA/CF microprocessor signals and bus conditions.

Various logic analyzers have different requirements for setup and hold times for their inputs of clocked (state) acquisitions. The 80960CA/CF also provides various setup and hold times for its outputs, and has requirements for its inputs. The HP E2432A provides a user-selectable choice of latches and clocking circuitry to ensure that these requirements for both the 80960CA/CF and the logic analyzers are met. The selection is made with Jumper J1 (see page 1-3).

Since the 80960CA/CF can operate in a pipelined bus mode, the HP E2432A provides circuitry to re-align the address, data, and status signals during pipelined bus cycles, so that pipeline skew is transparent to the logic analyzer. Pipelined bus accesses therefore only use a single state of logic analyzer acquisition storage, the same as non-pipelined accesses.

The HP E2432A filters states so that only valid data transfers get clocked into the logic analyzer. Wait states, idle states, and states where the 80960CA/CF is not the bus master are not clocked into the logic analyzer. However, the HP E2432A will clock the logic analyzer once at the beginning of HOLDA or BOFF# transactions, to indicate bus master changes. The duration of these transactions can be measured with logic analyzer time tags. Note that the HP 16540/16541A,D and HP 16542A support time tags up to 100 MHz (10 ns resolution); the other logic analyzers support time tags up to 16.67 MHz.

Since the 80960CA/CF is configurable in each of 16 memory regions, the HP E2432A must also be configured, and the inverse assembler must be initialized, to match and recognize the 80960CA/CF configuration (see pages 1-4 and 1-12). The logic analyzer then correctly displays the microprocessor activity according to the memory region configuration.

Only two of the six configurable items in the 80960CA/CF memory region need to be set in the HP E2432A; READY# /BTERM# enabling and bus pipeline enabling. Wait state configurations are taken care of, by looking at ADS# and BLAST# for Nxda wait states, and looking at the WAIT# signal for Nrad, Nrdd, Nwad, and Nwdd wait states. Bursting is handled automatically, since all of the address, data, and status signals are valid on the same PCLK rising edge. Bus size and byte-ordering information are extracted during inverse assembler initialization.

The following signals are not routed to the logic analyzer: DEN# , WAIT# , DT/R# , RESET# , PCLK1, PCLK2, CLKIN, and CLKMODE. These signals are either identical to other signals for clocked states, or have a constant value for clocked states.

Figure 3-1 shows the block diagram of the HP E2432A Preprocessor Interface.

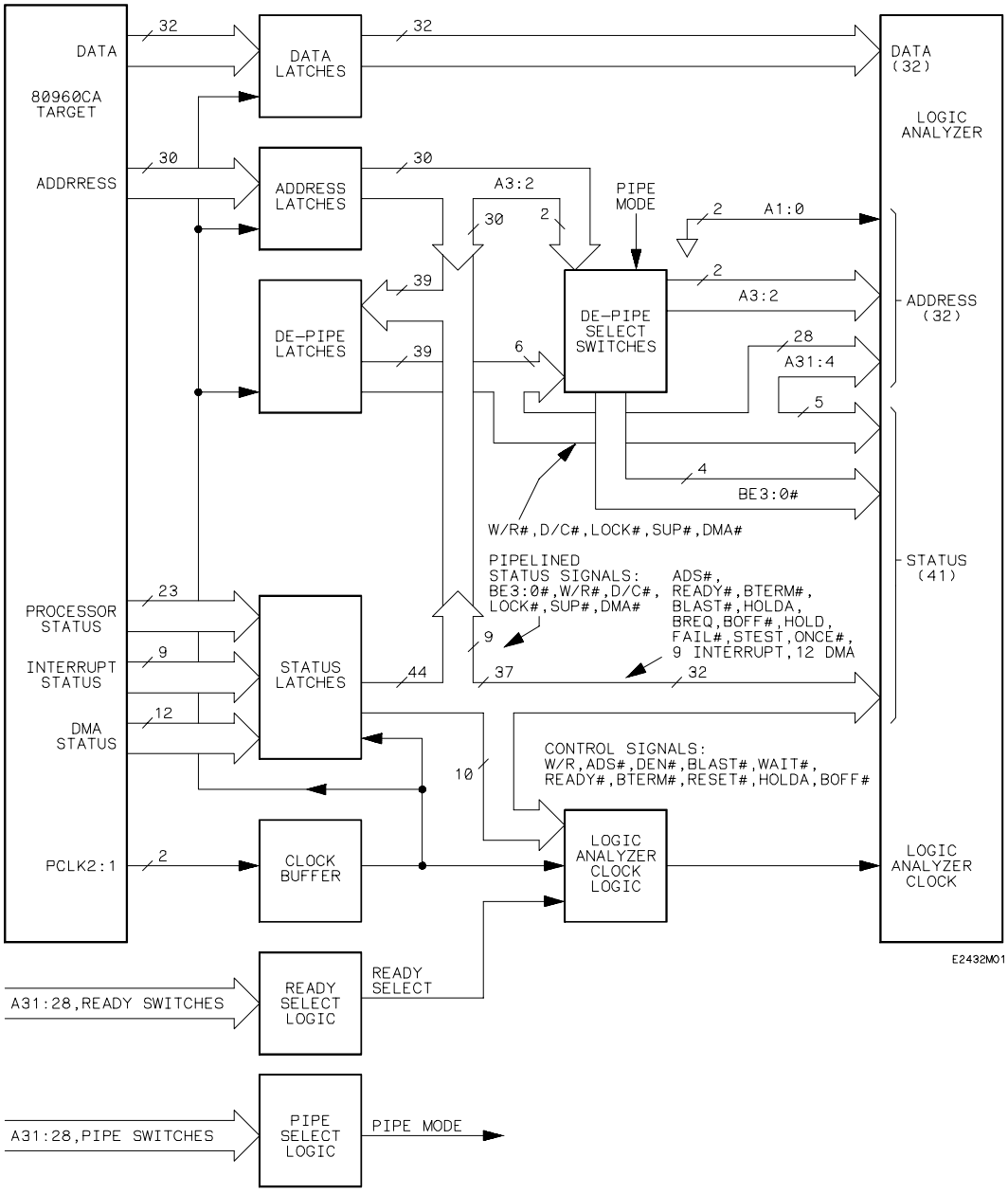

Figure 3-1. HP E2432A Block Diagram

Clocking

All 80960CA/CF system operation is referenced to the 80960CA/CF clock signals PCLK1 and PCLK2. The HP E2432A uses buffered versions of these two signals for its operation.

The preprocessor interface latches (samples) the microprocessor bus on every clock. If the access is a valid data transfer, a logic analyzer clock is generated within the setup/hold requirements selected by Jumper J1 (see page 1-3). During non-pipelined transfers, the de-pipe select switches will be set to the sample latch outputs. Note that these switches are actually active IC switches, and not the user-selectable discrete DIP switches.

Pipelined Accesses

The preprocessor interface will align pipelined bus transfers by latching the output of the sample latches into the de-pipe latches for signals that must be de-piped (A3:2 and BE3:0#). During pipelined transfers, the de-pipe select switches will be set to the de-pipe latch outputs. As above, for valid data transfers a logic analyzer clock is generated with the selected setup/hold requirements.

HOLDA and BOFF# Cycles

The preprocessor interface will generate a single logic analyzer clock at the start of a HOLDA or BOFF# cycle. This allows the user to see these cycles, without using more than one state of the logic analyzer memory.

Signals

The preprocessor interface sends the following signals to the logic analyzer: 32 address signals (A1 and A0 are tied to ground), 32 data signals, 20 microprocessor signals, nine interrupt controller signals, and 12 DMA signals. There are also seven user-definable TTL inputs on the preprocessor interface, which are latched the same way as the data signals. Some 80960CA/CF signals are not sent to the logic analyzer (see Interface Description).

Pipeline and READY# /BTERM# Enabling Switches

The pipeline and READY# /BTERM# enabling switches allow the preprocessor interface to de-pipe accesses, and to generate logic analyzer clocks based on READY# and BTERM# .

Logic Analyzer Clock Equation

The logic analyzer clock equation consists of several terms. The following is a list of the signals which are in the equation, and the required state for each signal (H = high, and L = low).

RESET# = H
and DEN# = L
WAIT# = H
Nxda# = H (not a Nxda wait state – based on ADS# and BLAST#)
READY# = L or BTERM# = L (depending on MRCT)
or
BOFF# = L and BOFF# last = H
HOLDA = H and HOLDA last = L
(this generates a single clock for BOFF# or HOLDA transaction)

80960CA/CF Signal to HP E2432A Connector Mapping

The following table describes the electrical interconnections implemented with the HP E2432A Preprocessor Interface. Since the pods on the logic analyzer may be numbered differently than the pods on the preprocessor interface, refer to table 1-2 to correlate the pod numbers.

Note

The interconnections implemented with the HP E2432A are not direct interconnections. The HP E2432A Preprocessor Interface places digital circuitry between the microprocessor pin and the logic analyzer input.

Table 3-1. 80960CA/CF Signal List

HP E2432A Connector	Preprocessor Pod	Preprocessor Probe	Microprocessor Pin Mnemonic	Microprocessor Pin Number	Label(s)
P1 (STAT_1)	1	CLK1	--	--	--
P1 (STAT_1)	1	0	BE0#	R9	STAT, BE
P1 (STAT_1)	1	1	BE1#	S7	STAT, BE
P1 (STAT_1)	1	2	BE2#	S6	STAT, BE
P1 (STAT_1)	1	3	BE3#	S5	STAT, BE
P1 (STAT_1)	1	4	W/R#	S10	STAT, W/R
P1 (STAT_1)	1	5	ADS#	R6	STAT, ADS
P1 (STAT_1)	1	6	READY#	S3	STAT, READY
P1 (STAT_1)	1	7	BTERM#	R4	STAT, BTERM
P1 (STAT_1)	1	8	D/C#	S13	STAT, D/C
P1 (STAT_1)	1	9	BLAST#	S8	STAT, BLAST
P1 (STAT_1)	1	10	LOCK#	S14	STAT, LOCK
P1 (STAT_1)	1	11	HOLDA	S4	STAT, HOLDA
P1 (STAT_1)	1	12	BREQ	R13	STAT, BREQ
P1 (STAT_1)	1	13	DMA#	R12	STAT, DMA
P1 (STAT_1)	1	14	SUP#	Q12	STAT, SUP
P1 (STAT_1)	1	15	BOFF#	B1	STAT, BOFF
P2 (DATA_L)	2	0	D0	E3	DATA
P2 (DATA_L)	2	1	D1	C2	DATA
P2 (DATA_L)	2	2	D2	D2	DATA
P2 (DATA_L)	2	3	D3	C1	DATA
P2 (DATA_L)	2	4	D4	E2	DATA
P2 (DATA_L)	2	5	D5	D1	DATA
P2 (DATA_L)	2	6	D6	F2	DATA
P2 (DATA_L)	2	7	D7	E1	DATA

Table 3-1. 80960CA/CF Signal List (Continued)

HP E2432A Connector	Preprocessor Pod	Preprocessor Probe	Microprocessor Pin Mnemonic	Microprocessor Pin Number	Label
P2 (DATA_L)	2	8	D8	F1	DATA
P2 (DATA_L)	2	9	D9	G1	DATA
P2 (DATA_L)	2	10	D10	H2	DATA
P2 (DATA_L)	2	11	D11	H1	DATA
P2 (DATA_L)	2	12	D12	J1	DATA
P2 (DATA_L)	2	13	D13	K1	DATA
P2 (DATA_L)	2	14	D14	L2	DATA
P2 (DATA_L)	2	15	D15	L1	DATA
P3 (DATA_H)	3	0	D16	M1	DATA
P3 (DATA_H)	3	1	D17	N1	DATA
P3 (DATA_H)	3	2	D18	N2	DATA
P3 (DATA_H)	3	3	D19	P1	DATA
P3 (DATA_H)	3	4	D20	P2	DATA
P3 (DATA_H)	3	5	D21	Q1	DATA
P3 (DATA_H)	3	6	D22	P3	DATA
P3 (DATA_H)	3	7	D23	Q2	DATA
P3 (DATA_H)	3	8	D24	R1	DATA
P3 (DATA_H)	3	9	D25	S1	DATA
P3 (DATA_H)	3	10	D26	Q3	DATA
P3 (DATA_H)	3	11	D27	R2	DATA
P3 (DATA_H)	3	12	D28	Q4	DATA
P3 (DATA_H)	3	13	D29	S2	DATA
P3 (DATA_H)	3	14	D30	Q5	DATA
P3 (DATA_H)	3	15	D31	R3	DATA

Table 3-1. 80960CA/CF Signal List (Continued)

HP E2432A Connector	Preprocessor Pod	Preprocessor Probe	Microprocessor Pin Mnemonic	Microprocessor Pin Number	Label
P4 (ADDR_L)	4	0	Vss	Note 1	ADDR
P4 (ADDR_L)	4	1	Vss	Note 1	ADDR
P4 (ADDR_L)	4	2	A2	D16	ADDR
P4 (ADDR_L)	4	3	A3	D17	ADDR
P4 (ADDR_L)	4	4	A4	E16	ADDR
P4 (ADDR_L)	4	5	A5	E17	ADDR
P4 (ADDR_L)	4	6	A6	F17	ADDR
P4 (ADDR_L)	4	7	A7	G16	ADDR
P4 (ADDR_L)	4	8	A8	G17	ADDR
P4 (ADDR_L)	4	9	A9	H17	ADDR
P4 (ADDR_L)	4	10	A10	J17	ADDR
P4 (ADDR_L)	4	11	A11	K17	ADDR
P4 (ADDR_L)	4	12	A12	L17	ADDR
P4 (ADDR_L)	4	13	A13	L16	ADDR
P4 (ADDR_L)	4	14	A14	M17	ADDR
P4 (ADDR_L)	4	15	A15	N17	ADDR
P5 (ADDR_H)	5	0	A16	N16	ADDR
P5 (ADDR_H)	5	1	A17	P17	ADDR
P5 (ADDR_H)	5	2	A18	Q17	ADDR
P5 (ADDR_H)	5	3	A19	P16	ADDR
P5 (ADDR_H)	5	4	A20	P15	ADDR
P5 (ADDR_H)	5	5	A21	Q16	ADDR
P5 (ADDR_H)	5	6	A22	R17	ADDR
P5 (ADDR_H)	5	7	A23	R16	ADDR

Note 1: Vss = C7, C8, C9, C10, C11, C12, F15, G3, G15, H3, H15, J3, J15, K3, K15, L3, L15, M3, M15, Q7, Q8, Q9, Q10, and Q11 (all tied together).

Table 3-1. 80960CA/CF Signal List (Continued)

HP E2432A Connector	Preprocessor Pod	Preprocessor Probe	Microprocessor Pin Mnemonic	Microprocessor Pin Number	Label
P5 (ADDR_H)	5	8	A24	Q15	ADDR
P5 (ADDR_H)	5	9	A25	S17	ADDR
P5 (ADDR_H)	5	10	A26	R15	ADDR
P5 (ADDR_H)	5	11	A27	S16	ADDR
P5 (ADDR_H)	5	12	A28	Q14	ADDR
P5 (ADDR_H)	5	13	A29	R14	ADDR
P5 (ADDR_H)	5	14	A30	Q13	ADDR
P5 (ADDR_H)	5	15	A31	S15	ADDR
P6 (STAT_2)	6	CLK1	--	--	--
P6 (STAT_2)	6	0	XINT0#	B15	XINT
P6 (STAT_2)	6	1	XINT1#	A15	XINT
P6 (STAT_2)	6	2	XINT2#	A17	XINT
P6 (STAT_2)	6	3	XINT3#	B16	XINT
P6 (STAT_2)	6	4	XINT4#	C15	XINT
P6 (STAT_2)	6	5	XINT5#	B17	XINT
P6 (STAT_2)	6	6	XINT6#	C16	XINT
P6 (STAT_2)	6	7	XINT7#	C17	XINT
P6 (STAT_2)	6	8	NMI#	D15	NMI
P6 (STAT_2)	6	9	HOLD	R5	HOLD
P6 (STAT_2)	6	10	FAIL#	A2	FAIL
P6 (STAT_2)	6	11	STEST	B2	STEST
P6 (STAT_2)	6	12	ONCE#	C3	ONCE
P6 (STAT_2)	6	13	--	--	EXTERN
P6 (STAT_2)	6	14	--	--	EXTERN
P6 (STAT_2)	6	15	--	--	EXTERN

Table 3-1. 80960CA/CF Signal List (Continued)

HP E2432A Connector	Preprocessor Pod	Preprocessor Probe	Microprocessor Pin Mnemonic	Microprocessor Pin Number	Label
P7 (STAT_3)	7	0	DREQ0#	B5	DREQ
P7 (STAT_3)	7	1	DREQ1#	A6	DREQ
P7 (STAT_3)	7	2	DREQ2#	B6	DREQ
P7 (STAT_3)	7	3	DREQ3#	A7	DREQ
P7 (STAT_3)	7	4	DACK0#	B8	DACK
P7 (STAT_3)	7	5	DACK1#	A8	DACK
P7 (STAT_3)	7	6	DACK2#	A9	DACK
P7 (STAT_3)	7	7	DACK3#	A10	DACK
P7 (STAT_3)	7	8	EOP0# /TC0#	A11	EOP/TC
P7 (STAT_3)	7	9	EOP1# /TC1#	A12	EOP/TC
P7 (STAT_3)	7	10	EOP2# /TC2#	A13	EOP/TC
P7 (STAT_3)	7	11	EOP3# /TC3#	A14	EOP/TC
P7 (STAT_3)	7	12	--	--	EXTERN
P7 (STAT_3)	7	13	--	--	EXTERN
P7 (STAT_3)	7	14	--	--	EXTERN
P7 (STAT_3)	7	15	--	--	EXTERN

Note: The following signals are not routed to the logic analyzer: DT/R# (S11), DEN# (S9), WAIT# (S12), RESET# (A16), PCLK1 (B14), PCLK2 (B13), CLKIN (C13), and CLKMODE (C14).

Vcc = B7, B8, B10, B11, B12, C6, E15, F3, F16, G2, H16, J2, J16, K2, K16, M2, M16, N3, N15, Q6, R7, R8, R10, and R11. These are unconnected.

NC (no connect) = A1, A3, A4, A5, B3, B4, C4, C5, and D3. These are unconnected.

Servicing

The repair strategy for the HP E2432A is board replacement. Table 3-2 lists the mechanical parts that may be replaced if they are damaged or lost. Contact your nearest Hewlett-Packard Sales/Service Office for further information on servicing the board.

Exchange assemblies are available when a repairable assembly is returned to Hewlett-Packard. These assemblies have been set up on the "Exchange Assembly" program. This allows you to exchange a faulty assembly with one that has been repaired, calibrated, and performance verified by the factory. The cost is significantly less than that of a new assembly.

Table 3-2. Replaceable Parts

HP Part Number	Description
E2432-69501	Exchange Board/Cable Assembly
E2432-68703	Inverse Assembler Disk Pouch
E2432-66501	Circuit Board/Cable Assembly
1200-1512	Pin Protector
01650-63204	Termination Module

Dimensions

Figure 3-2 lists the dimensions for the HP E2432A circuit board. The dimensions are listed in inches (millimeters).

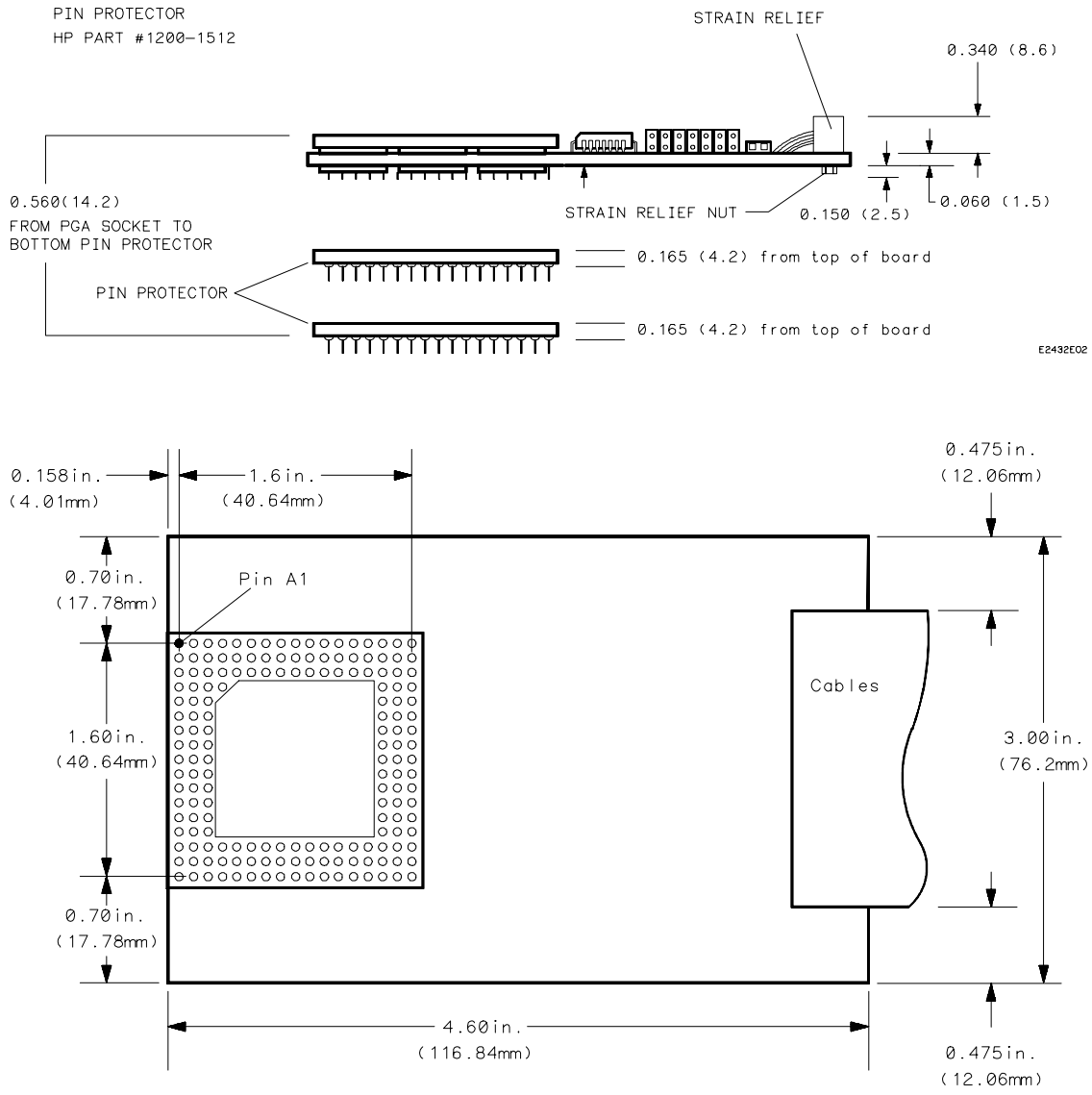

Figure 3-2. HP E2432A Dimensions - inches (mm)

A

Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes " ". Symptoms are listed without quotes.

If you are still having difficulties after trying the suggestions below, please contact your local Hewlett-Packard service center for additional assistance.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, the microprocessor or the preprocessor interface are not installed properly, or they are not making electrical contact.

- Verify that the microprocessor and the preprocessor interface are properly rotated and aligned.
- Verify that the microprocessor and the preprocessor interface are securely inserted into their respective sockets.
- Verify that the logic analyzer cables are in the proper sockets of the preprocessor interface and firmly inserted.
- Reduce the number of extender sockets (see also "Capacitive Loading").
- Ensure that there is power from the logic analyzer to the preprocessor interface.

"Slow or Missing Clock"

This error message might occur if the logic analyzer cards are not firmly seated in the HP 16500A/16501A frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check the that the logic analyzer pods are connected to the proper connectors, as listed in table 1-2. For HP 1650A and HP 16510A Logic Analyzers, check the preprocessor interface power fuse in the logic analyzer.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500A disk operation menu. Selecting Load {All} will cause incorrect operation when loading preprocessor interface configuration files.

"Selected File is Incompatible"

The logic analyzer displays this message if you try to load a configuration file for the wrong module. Ensure that you are loading the appropriate configuration file for your logic analyzer.

". . . Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler file is not renamed or deleted. Note that in some instances you will want to rename the inverse assembler (see page 1-13).

No Inverse Assembly

Ensure that the inverse assembler has been initialized (see Chapter 1). Also, verify that the inverse assembler has been synchronized by placing an opcode at the top of the display and pressing the Invasm key (see "Inverse Assembler" in Chapter 2).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.
- Verify that the instruction cache has been disabled.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

On the HP 1650A, HP 1651A, and HP 16510A Logic Analyzers if there is no activity the fuse which allows power to the preprocessor interface is probably blown. Check the fuse in the logic analyzer. On the other logic analyzers, if there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading.

One technique to reduce the capacitive loading is to remove as many pin protectors, extenders, and adapters as possible. If a passive preprocessor interface is available, try using that instead of an active one.

"State Clock Violates Overdrive Specification"

At least one 16-channel pod in the state analysis measurement stored a different number of states before trigger than the other pods. This is usually caused by sending a clocking signal to the state analyzer that does not meet all of the specified conditions, such as minimum period, minimum pulse width, or minimum amplitude. Poor pulse shaping could also cause this problem. Check the target PCLK pulse shape for potential false clocking. Also, refer to table 2-1 on page 2-2 for maximum bus rates.

Note 

The error message "State Clock Violates Overdrive Specification" should only occur for HP 1650A,B, HP 1652B, HP 16510A,B, and HP 16511B Logic Analyzers with the Clock Period field set to < 60 ns. If this error message is observed with the Clock Period set to > 60 ns, you may have a faulty logic analyzer. If a failure is suspected in your logic analyzer, contact your nearest Hewlett-Packard Sales/Service Office for information on servicing the instrument.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted prefetches or cache line fills. Add the prefetch queue depth to the trigger address to avoid this problem.

"Waiting for Trigger"

If a trigger pattern is specified, this message indicates that the specified trigger pattern did not occur. Verify that the triggering pattern is correctly set.

If a "don't care" trigger condition is set for an HP 16511B Logic Analyzer, this message indicates only one of the two cards is receiving its state clock. Refer to "Slow or Missing Clock."

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

Bent Pins

Bent pins on the preprocessor interface, pin protectors, or adapters can cause system errors or inverse assembly errors. Ensure all pins are properly aligned and making contact.

"Time from Arm Greater Than 41.93 ms."

The state/timing analyzers have a counter to keep track of the time from when an analyzer is armed to when it triggers. The width and clock rate of this counter allow it to count for up to 41.93 ms before it overflows. Once the counter has overflowed, the system does not have the data it needs to calculate the time between module triggers. The system must know this time to be able to display data from multiple modules on a single screen.

No Setup/Hold Field on Format Screen

The HP 16540/16541A,D or HP 16542A Logic Analyzer cards are not calibrated. Refer to your logic analyzer reference manual for procedures to calibrate the cards.

"Default Calibration Factors Loaded" (16540/41/42)

The default calibration file for the logic analyzer was loaded. The logic analyzer must be calibrated when using HP 16540A,D, HP 16541A,D or HP 16542A cards. Refer to your logic analyzer manual for procedures to calibrate the master clocking system, and ensure that the "cal factors" file is saved.